```
RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940;  selected revisions: 27
description:
top level BOM
----------------------------
revision 3.680
date: 1995/05/05 04:18:31;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

at/atdisallowxc.pla:
  Target cases were using the gateway permission field instead of the execute
  field.  No cell names changed, so placement still works.
  Test nullTest_pl noticed.  This will probably fix but examination
  of UU exception priorities and preempts is beginning next.
----------------------------
revision 3.679
date: 1995/05/05 02:40:41;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc


Consolidating recent placement tweaks into .0 BOM.  This version
should place completely at the top level on the first iteration.

Pick up latest top level files:

Makefile.tst
Makefile.vo
genpim2.pl

New drio.power.tab.top in drio section
----------------------------
revision 3.678
date: 1995/05/04 23:11:25;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

fix dc/timing problem with GIhit2CR10_N
----------------------------
revision 3.677
date: 1995/05/04 22:35:29;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

Slight adjustment of placement and power levels to:
1) avoid collisions when u150's on right side power up.
2) reduce absolute sofa clock to output delays.
----------------------------
revision 3.676
date: 1995/05/04 19:29:37;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/au

avoid toplevel collisions
```

```
----------------------------
revision 3.675
date: 1995/05/04 17:23:03;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cp

avoid toplevel collisions
----------------------------
revision 3.674
date: 1995/05/04 16:25:10;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

Places rightmost block of flops up against CR and right justifies
so they can grow to the left (u150 cells should grow, they drive
cross-chip wires).
----------------------------
revision 3.673
date: 1995/05/04 07:34:42;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
cj/rsrvd.tst:  AUndx1500 now stops at bit 2.
euterpe.status:  Reduce note on sub-octlet stores not illegal to sys reg only.
  Delete fixed bug on nonblocking illegal loads for sych ops and bgate.
icc/icc.pim.txt:  Move big rstOut flop up to new row borrowed from CJ since
  dickson getting collision with IFe at top level.
----------------------------
revision 3.672
date: 1995/05/04 04:33:53;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/icc

avoid toplevel collisions
----------------------------
revision 3.671
date: 1995/05/04 04:31:55;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

avoid top level collisons and deconjest control stripe
----------------------------
revision 3.670
date: 1995/05/04 04:29:59;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions
----------------------------
revision 3.669
date: 1995/05/04 00:26:25;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/nb

releasing better power.tab.top
----------------------------
revision 3.668
```

```
date: 1995/05/03 23:25:12;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

avoid toplevel collisions with mc
----------------------------
revision 3.667
date: 1995/05/03 23:12:21;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

at.V: Inhibited the xcLva freeze on dcacheMiss and on gtlb and tdNdx (CC ndx)
conflicts.

at.pim: updated placement.

dcacheharder_woody_V fabbed.
----------------------------
revision 3.666
date: 1995/05/03 16:54:44;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

New drio placement.  New file drio.nearpads.pim.
----------------------------
revision 3.665
date: 1995/05/03 02:07:10;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/ukernel

name of kernel changed (hwsimkernel instead of kernel.nocalliope) and rules to
make .lst files
----------------------------
revision 3.664
date: 1995/05/03 01:51:34;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify
      Makerules.local

SOFT_BUILD needs to keep it's own COPT
----------------------------
revision 3.663
date: 1995/05/02 23:36:14;  author: vo;  state: Exp;  lines: +2 -2
Release Target: euterpe/baseplate
      custom.pif

moved all xb cell placement to verilog/bsrc/genpim2.pl .
----------------------------
revision 3.662
date: 1995/05/02 22:00:42;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cc

right justify rightmost section of layout
----------------------------
revision 3.661
date: 1995/05/02 03:05:59;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

aviod toplevel collisions with cc
----------------------------
revision 3.660
date: 1995/05/01 22:26:40;  author: woody;  state: Exp;  lines: +2 -2
```

```
Release Target: euterpe/verilog/bsrc

euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 3.659
date: 1995/05/01 04:02:29;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

at/at.V:
  Forgot to hook up this inside at.V; discovered placement no worse than before.
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
----------------------------
revision 3.658
date: 1995/05/01 03:54:35;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.V at/at.V uu/uu_control.pim:
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
  AT placement not updated but I think it was already not usable.
uu/uumemuv.tdcd:  Comment:  explain why we don't improve the espresso phase.
uu/uumemuv.tdcd:  Only hexlet stores were legal to NB; add octlet stores.
{cj,ife,tst}/*?rst.tst:  CPrdibtreq23 & CPwtibtreq5 were missing.
tst/drvchk.V:  Reg bypassing AUndx around SR pointing at stale name.
tst/job.tst:  Mask & div4 reversed for NB case of AUndx1500cR2.
euterpe.status:  CDIO fixed its write-hi-data-in hold violation a long time ago.
uu/uustepuu.pla:  Lessen confusion in comments on split-write ops (GGFMul/ExtrI)
----------------------------
revision 3.657
date: 1995/04/30 18:03:13;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt


Tau fannout fix.
----------------------------
revision 3.656
date: 1995/04/30 17:54:43;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

pick up genptab.pl for swing force
----------------------------
revision 3.655
date: 1995/04/30 17:14:38;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/io

turn packing back on for io1
----------------------------
revision 3.654
```

```
date: 1995/04/29 23:02:16;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc


Releasing at.V

----------------------------
revision 1.56
date: 1995/04/29 13:35:55 LT;  author: woody;  state: Exp;  lines: +4 -6
Wrong again! access type *is* required in nbHiPri bit. It is needed
to sift out the gtlbHit=X cases, such as SN64WRIQ.
----------------------------
revision 1.55
date: 1995/04/29 13:12:32 LT;  author: woody;  state: Exp;  lines: +6 -2
Fix X problem with nbHiPriR11. When the logic was removed from atprchk
gtlbHit was inadvertantly left off. NrmlMem also was removed from the equation
but that was intentional, see comment in at.V for explanation.
----------------------------
=============================================================================

RCS file: /s6/cvsroot/euterpe/baseplate/BOM,v
Working file: baseplate/BOM
head: 33.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 65;    selected revisions: 1
description:
releasebom adding BOM
----------------------------
revision 22.1
date: 1995/05/02 23:35:55;  author: vo;  state: Exp;  lines: +2 -2
Release Target: euterpe/baseplate
      custom.pif

moved all xb cell placement to verilog/bsrc/genpim2.pl .
=============================================================================

RCS file: /s6/cvsroot/euterpe/baseplate/custom.pif,v
Working file: baseplate/custom.pif
head: 3.22
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 22;    selected revisions: 1
description:
----------------------------
revision 3.21
date: 1995/05/02 23:28:10;  author: vo;  state: Exp;  lines: +0 -4
moved xb cells to bsrc/genpim2.pl
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Makefile,v
Working file: doc/Makefile
head: 4.12
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 2
description:
initial version
----------------------------
revision 4.10
date: 1995/05/02 15:57:38;  author: bobm;  state: Exp;  lines: +2 -2
Added a missing word.
----------------------------
revision 4.9
date: 1995/05/01 15:59:26;  author: bobm;  state: Exp;  lines: +3 -2
Added endian.mif appendix.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/cerberus.mif,v
Working file: doc/cerberus.mif
head: 4.39
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 53;    selected revisions: 2
description:
----------------------------
revision 4.33
date: 1995/05/02 00:44:52;  author: bobm;  state: Exp;  lines: +52 -52
Last review comments incorporated before book review.
----------------------------
revision 4.32
date: 1995/04/29 23:31:46;  author: bobm;  state: Exp;  lines: +4795 -1741
Checkin of some review changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/clock.mif,v
Working file: doc/clock.mif
head: 19.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 2
description:
----------------------------
revision 19.3
date: 1995/05/02 00:44:15;  author: bobm;  state: Exp;  lines: +62 -62
Last review comments incorporated before book review.
----------------------------
revision 19.2
date: 1995/04/29 23:31:26;  author: bobm;  state: Exp;  lines: +21965 -123
Checkin of some review changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/endian.mif,v
Working file: doc/endian.mif
```

```
head: 19.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 2
description:
----------------------------
revision 19.2
date: 1995/05/02 00:45:31;  author: bobm;  state: Exp;  lines: +103 -103
Last review comments incorporated before book review.
----------------------------
revision 19.1
date: 1995/04/29 23:32:30;  author: bobm;  state: Exp;
Checkin of some review changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/euterpe-microarchTOC.mif,v
Working file: doc/euterpe-microarchTOC.mif
head: 4.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 22;    selected revisions: 2
description:
----------------------------
revision 4.12
date: 1995/05/02 00:20:17;  author: bobm;  state: Exp;  lines: +6629 -308
Last review comments incorporated before book review.
----------------------------
revision 4.11
date: 1995/04/29 23:28:22;  author: bobm;  state: Exp;  lines: +219 -157
Checkin of some review changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/events.mif,v
Working file: doc/events.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28;    selected revisions: 2
description:
----------------------------
revision 4.20
date: 1995/05/02 00:43:50;  author: bobm;  state: Exp;  lines: +193 -60
Last review comments incorporated before book review.
----------------------------
revision 4.19
date: 1995/04/29 23:31:14;  author: bobm;  state: Exp;  lines: +6341 -215
Checkin of some review changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/front.mif,v
Working file: doc/front.mif
```

```
head: 16.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 16.6
date: 1995/05/02 00:20:09;  author: bobm;  state: Exp;  lines: +41 -26
Last review comments incorporated before book review.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/intro.mif,v
Working file: doc/intro.mif
head: 4.22
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 2
description:
----------------------------
revision 4.19
date: 1995/05/02 00:20:25;  author: bobm;  state: Exp;  lines: +115 -115
Last review comments incorporated before book review.
----------------------------
revision 4.18
date: 1995/04/29 23:28:26;  author: bobm;  state: Exp;  lines: +143 -185
Checkin of some review changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/memory.mif,v
Working file: doc/memory.mif
head: 4.36
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46;    selected revisions: 2
description:
----------------------------
revision 4.30
date: 1995/05/02 00:22:23;  author: bobm;  state: Exp;  lines: +15896 -11249
Last review comments incorporated before book review.
----------------------------
revision 4.29
date: 1995/04/29 23:29:35;  author: bobm;  state: Exp;  lines: +2567 -9740
Checkin of some review changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/newchanges.mif,v
Working file: doc/newchanges.mif
head: 16.13
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 13;    selected revisions: 2
description:
----------------------------
revision 16.8
date: 1995/05/02 00:45:40;  author: bobm;  state: Exp;  lines: +78 -33
Last review comments incorporated before book review.
----------------------------
revision 16.7
date: 1995/04/29 23:32:33;  author: bobm;  state: Exp;  lines: +117 -50
Checkin of some review changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/opcodes.mif,v
Working file: doc/opcodes.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 39;    selected revisions: 2
description:
----------------------------
revision 4.21
date: 1995/05/02 00:20:58;  author: bobm;  state: Exp;  lines: +31 -31
Last review comments incorporated before book review.
----------------------------
revision 4.20
date: 1995/04/29 23:28:43;  author: bobm;  state: Exp;  lines: +29 -54
Checkin of some review changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/pipeline.mif,v
Working file: doc/pipeline.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 27;    selected revisions: 2
description:
----------------------------
revision 4.19
date: 1995/05/02 00:22:01;  author: bobm;  state: Exp;  lines: +153 -153
Last review comments incorporated before book review.
----------------------------
revision 4.18
date: 1995/04/29 23:29:10;  author: bobm;  state: Exp;  lines: +9681 -3249
Checkin of some review changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/reset.mif,v
Working file: doc/reset.mif
head: 4.22
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 26;    selected revisions: 2
description:
----------------------------
revision 4.19
date: 1995/05/02 00:44:03;  author: bobm;  state: Exp;  lines: +50 -28
Last review comments incorporated before book review.
----------------------------
revision 4.18
date: 1995/04/29 23:31:21;  author: bobm;  state: Exp;  lines: +290 -262
Checkin of some review changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/verify.html,v
Working file: doc/verify.html
head: 18.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
----------------------------
revision 18.15
date: 1995/05/02 18:50:37;  author: doi;  state: Exp;  lines: +5 -1
describe additional functionality for the "forward-only-active" keyword
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;   selected revisions: 2
description:
----------------------------
revision 4.106
date: 1995/05/03 02:06:46;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/ukernel

name of kernel changed (hwsimkernel instead of kernel.nocalliope) and rules to
make .lst files
----------------------------
revision 4.105
date: 1995/05/03 01:51:09;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify
      Makerules.local

SOFT_BUILD needs to keep it's own COPT
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/Makerules.local,v
Working file: verify/Makerules.local
head: 3.16
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 1
description:
----------------------------
revision 3.12
date: 1995/05/03 01:50:45;  author: doi;  state: Exp;  lines: +5 -1
SOFT_BUILD needs to keep it's own COPT
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/event/Makefile,v
Working file: verify/obj/processor/event/Makefile
head: 1.63
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 63;    selected revisions: 1
description:
----------------------------
revision 1.62
date: 1995/05/04 05:46:53;  author: jeffm;  state: Exp;  lines: +2 -2
Added smux to reserved ops - conditioned with NOSMUX flag.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v
Working file: verify/obj/processor/inst/Makefile
head: 1.182
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 4
description:
----------------------------
revision 1.152
date: 1995/05/04 23:55:06;  author: jeffm;  state: Exp;  lines: +2 -2
Try to recreate failure seen with nullTest - page cross interfering
with branch target exception handling.
----------------------------
revision 1.151
date: 1995/05/03 23:49:22;  author: jeffm;  state: Exp;  lines: +2 -2
New test - checks page crosser scenarios.
----------------------------
revision 1.150
date: 1995/05/01 22:57:44;  author: jeffm;  state: Exp;  lines: +2 -2
Test uncached bgate, synch ops, and illegal sizes of uncached stores.
Since terp does not support these exception cases yet, the test
is untested.
----------------------------
revision 1.149
date: 1995/05/01 21:50:22;  author: jeffm;  state: Exp;  lines: +2 -2
New test - check gtlb setup where only write access is available, not
read access.
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verify/perf/cerb_perf.S,v
Working file: verify/perf/cerb_perf.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 1.3
date: 1995/05/03 22:58:36;  author: claseman;  state: Exp;  lines: +7 -5
use octlet 6 instead of octlet 8
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgcompressispc1.test,v
Working file: verify/standalone/dp/dpgcompressispc1.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:40:17;  author: veena;  state: Exp;  lines: +15 -15
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgcompressispc16.test,v
Working file: verify/standalone/dp/dpgcompressispc16.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:40:19;  author: veena;  state: Exp;  lines: +1 -1
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgcompressispc2.test,v
Working file: verify/standalone/dp/dpgcompressispc2.test
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 2
description:
----------------------------
revision 2.3
date: 1995/05/01 17:46:22;  author: veena;  state: Exp;  lines: +1 -1
```

```
didn't remove one exception case.
----------------------------
revision 2.2
date: 1995/04/29 22:40:20;  author: veena;  state: Exp;  lines: +14 -14
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgcompressispc4.test,v
Working file: verify/standalone/dp/dpgcompressispc4.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:40:22;  author: veena;  state: Exp;  lines: +10 -10
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgcompressispc8.test,v
Working file: verify/standalone/dp/dpgcompressispc8.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:40:24;  author: veena;  state: Exp;  lines: +3 -3
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgexpandispc1.test,v
Working file: verify/standalone/dp/dpgexpandispc1.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:37:05;  author: veena;  state: Exp;  lines: +21 -21
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgexpandispc16.test,v
Working file: verify/standalone/dp/dpgexpandispc16.test
head: 2.2
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:37:06;  author: veena;  state: Exp;  lines: +28 -28
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgexpandispc2.test,v
Working file: verify/standalone/dp/dpgexpandispc2.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:37:08;  author: veena;  state: Exp;  lines: +23 -23
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgexpandispc32.test,v
Working file: verify/standalone/dp/dpgexpandispc32.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:37:10;  author: veena;  state: Exp;  lines: +43 -43
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgexpandispc4.test,v
Working file: verify/standalone/dp/dpgexpandispc4.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:37:11;  author: veena;  state: Exp;  lines: +19 -19
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgexpandispc8.test,v
Working file: verify/standalone/dp/dpgexpandispc8.test
```

```
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:37:13;  author: veena;  state: Exp;  lines: +13 -13
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgmshrispc16.test,v
Working file: verify/standalone/dp/dpgmshrispc16.test
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/04/29 22:35:21;  author: veena;  state: Exp;  lines: +17 -17
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgmshrispc2.test,v
Working file: verify/standalone/dp/dpgmshrispc2.test
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/04/29 22:35:23;  author: veena;  state: Exp;  lines: +25 -25
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgmshrispc32.test,v
Working file: verify/standalone/dp/dpgmshrispc32.test
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/04/29 22:35:25;  author: veena;  state: Exp;  lines: +34 -34
removed exception cases, now they are tested in uu.
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgmshrispc4.test,v
Working file: verify/standalone/dp/dpgmshrispc4.test
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/04/29 22:35:27;  author: veena;  state: Exp;  lines: +15 -15
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgmshrispc64.test,v
Working file: verify/standalone/dp/dpgmshrispc64.test
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/04/29 22:35:29;  author: veena;  state: Exp;  lines: +67 -67
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgmshrispc8.test,v
Working file: verify/standalone/dp/dpgmshrispc8.test
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/04/29 22:35:32;  author: veena;  state: Exp;  lines: +11 -11
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgrotrispc16.test,v
Working file: verify/standalone/dp/dpgrotrispc16.test
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
```

```
date: 1995/05/01 17:45:15;  author: veena;  state: Exp;  lines: +17 -17
forgot to checkin this. Removed exception cases.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgrotrispc2.test,v
Working file: verify/standalone/dp/dpgrotrispc2.test
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/05/01 17:45:18;  author: veena;  state: Exp;  lines: +25 -25
forgot to checkin this. Removed exception cases.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgrotrispc32.test,v
Working file: verify/standalone/dp/dpgrotrispc32.test
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/05/01 17:45:20;  author: veena;  state: Exp;  lines: +33 -33
forgot to checkin this. Removed exception cases.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgrotrispc4.test,v
Working file: verify/standalone/dp/dpgrotrispc4.test
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/05/01 17:45:22;  author: veena;  state: Exp;  lines: +15 -15
forgot to checkin this. Removed exception cases.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgrotrispc64.test,v
Working file: verify/standalone/dp/dpgrotrispc64.test
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
```

```
description:
----------------------------
revision 4.2
date: 1995/05/01 17:45:26;  author: veena;  state: Exp;  lines: +69 -69
forgot to checkin this. Removed exception cases.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgrotrispc8.test,v
Working file: verify/standalone/dp/dpgrotrispc8.test
head: 4.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/05/01 17:45:28;  author: veena;  state: Exp;  lines: +11 -11
forgot to checkin this. Removed exception cases.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgshlispc16.test,v
Working file: verify/standalone/dp/dpgshlispc16.test
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/29 22:36:04;  author: veena;  state: Exp;  lines: +17 -17
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgshlispc2.test,v
Working file: verify/standalone/dp/dpgshlispc2.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:36:05;  author: veena;  state: Exp;  lines: +16 -16
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgshlispc32.test,v
Working file: verify/standalone/dp/dpgshlispc32.test
head: 1.4
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/29 22:36:07;  author: veena;  state: Exp;  lines: +33 -33
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgshlispc4.test,v
Working file: verify/standalone/dp/dpgshlispc4.test
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/29 22:36:09;  author: veena;  state: Exp;  lines: +15 -15
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgshlispc64.test,v
Working file: verify/standalone/dp/dpgshlispc64.test
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/29 22:36:10;  author: veena;  state: Exp;  lines: +69 -69
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgshlispc8.test,v
Working file: verify/standalone/dp/dpgshlispc8.test
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/29 22:36:12;  author: veena;  state: Exp;  lines: +11 -11
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgshrispc16.test,v
Working file: verify/standalone/dp/dpgshrispc16.test
```

```
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/29 22:32:15;  author: veena;  state: Exp;  lines: +17 -17
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgshrispc2.test,v
Working file: verify/standalone/dp/dpgshrispc2.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:32:17;  author: veena;  state: Exp;  lines: +16 -16
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgshrispc32.test,v
Working file: verify/standalone/dp/dpgshrispc32.test
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/29 22:32:19;  author: veena;  state: Exp;  lines: +33 -33
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgshrispc4.test,v
Working file: verify/standalone/dp/dpgshrispc4.test
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/29 22:32:21;  author: veena;  state: Exp;  lines: +15 -15
removed exception cases, now they are tested in uu.
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgshrispc64.test,v
Working file: verify/standalone/dp/dpgshrispc64.test
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/29 22:32:23;  author: veena;  state: Exp;  lines: +69 -69
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgshrispc8.test,v
Working file: verify/standalone/dp/dpgshrispc8.test
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/29 22:32:25;  author: veena;  state: Exp;  lines: +11 -11
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgucompressispc1.test,v
Working file: verify/standalone/dp/dpgucompressispc1.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:40:52;  author: veena;  state: Exp;  lines: +15 -15
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgucompressispc16.test,v
Working file: verify/standalone/dp/dpgucompressispc16.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
```

```
date: 1995/04/29 22:40:54;  author: veena;  state: Exp;  lines: +1 -1
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgucompressispc2.test,v
Working file: verify/standalone/dp/dpgucompressispc2.test
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 2
description:
----------------------------
revision 2.3
date: 1995/05/01 17:46:19;  author: veena;  state: Exp;  lines: +1 -1
didn't remove one exception case.
----------------------------
revision 2.2
date: 1995/04/29 22:40:56;  author: veena;  state: Exp;  lines: +14 -14
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgucompressispc4.test,v
Working file: verify/standalone/dp/dpgucompressispc4.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:40:58;  author: veena;  state: Exp;  lines: +10 -10
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgucompressispc8.test,v
Working file: verify/standalone/dp/dpgucompressispc8.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:41:00;  author: veena;  state: Exp;  lines: +3 -3
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpguexpandispc1.test,v
Working file: verify/standalone/dp/dpguexpandispc1.test
head: 2.2
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:37:43;  author: veena;  state: Exp;  lines: +21 -21
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpguexpandispc16.test,v
Working file: verify/standalone/dp/dpguexpandispc16.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:37:45;  author: veena;  state: Exp;  lines: +28 -28
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpguexpandispc2.test,v
Working file: verify/standalone/dp/dpguexpandispc2.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:37:47;  author: veena;  state: Exp;  lines: +23 -23
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpguexpandispc32.test,v
Working file: verify/standalone/dp/dpguexpandispc32.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:37:49;  author: veena;  state: Exp;  lines: +43 -43
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpguexpandispc4.test,v
```

```
Working file: verify/standalone/dp/dpguexpandispc4.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:37:51;  author: veena;  state: Exp;  lines: +19 -19
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpguexpandispc8.test,v
Working file: verify/standalone/dp/dpguexpandispc8.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:37:53;  author: veena;  state: Exp;  lines: +13 -13
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgushrispc16.test,v
Working file: verify/standalone/dp/dpgushrispc16.test
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/29 22:33:19;  author: veena;  state: Exp;  lines: +17 -17
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgushrispc2.test,v
Working file: verify/standalone/dp/dpgushrispc2.test
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/04/29 22:33:22;  author: veena;  state: Exp;  lines: +16 -16
removed exception cases, now they are tested in uu.
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgushrispc32.test,v
Working file: verify/standalone/dp/dpgushrispc32.test
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/29 22:33:24;  author: veena;  state: Exp;  lines: +33 -33
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgushrispc4.test,v
Working file: verify/standalone/dp/dpgushrispc4.test
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/29 22:33:25;  author: veena;  state: Exp;  lines: +15 -15
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgushrispc64.test,v
Working file: verify/standalone/dp/dpgushrispc64.test
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/04/29 22:33:27;  author: veena;  state: Exp;  lines: +69 -69
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/dp/dpgushrispc8.test,v
Working file: verify/standalone/dp/dpgushrispc8.test
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
```

```
revision 1.4
date: 1995/04/29 22:33:30;  author: veena;  state: Exp;  lines: +11 -11
removed exception cases, now they are tested in uu.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/Makefile,v
Working file: verify/standalone/uu/Makefile
head: 1.62
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 62;    selected revisions: 1
description:
----------------------------
revision 1.62
date: 1995/05/04 05:46:53;  author: jeffm;  state: Exp;  lines: +2 -2
Added smux to reserved ops - conditioned with NOSMUX flag.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/Attic/exresmajor.S,v
Working file: verify/standalone/uu/exresmajor.S
head: 2.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 2.7
date: 1995/05/04 05:46:55;  author: jeffm;  state: Exp;  lines: +6 -2
Added smux to reserved ops - conditioned with NOSMUX flag.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/Attic/exressminortest.S,v
Working file: verify/standalone/uu/exressminortest.S
head: 2.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 2.5
date: 1995/05/04 05:46:58;  author: jeffm;  state: Exp;  lines: +5 -1
Added smux to reserved ops - conditioned with NOSMUX flag.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v
Working file: verify/toplevel/Makefile
head: 1.185
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 185;   selected revisions: 4
description:
----------------------------
revision 1.152
date: 1995/05/04 23:55:06;  author: jeffm;  state: Exp;  lines: +2 -2
Try to recreate failure seen with nullTest - page cross interfering
with branch target exception handling.
----------------------------
revision 1.151
date: 1995/05/03 23:49:22;  author: jeffm;  state: Exp;  lines: +2 -2
New test - checks page crosser scenarios.
----------------------------
revision 1.150
date: 1995/05/01 22:57:44;  author: jeffm;  state: Exp;  lines: +2 -2
Test uncached bgate, synch ops, and illegal sizes of uncached stores.
Since terp does not support these exception cases yet, the test
is untested.
----------------------------
revision 1.149
date: 1995/05/01 21:50:22;  author: jeffm;  state: Exp;  lines: +2 -2
New test - check gtlb setup where only write access is available, not
read access.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/brcrosstest.S,v
Working file: verify/toplevel/brcrosstest.S
head: 35.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 3
description:
----------------------------
revision 35.3
date: 1995/05/04 22:29:14;  author: jeffm;  state: Exp;  lines: +3 -3
Shortened cylinder 4's case - it was several times longer than any
other cylinder's.
----------------------------
revision 35.2
date: 1995/05/04 22:16:25;  author: jeffm;  state: Exp;  lines: +3 -3
Test bug - cyl1 jumped into cyl0's loop.
----------------------------
revision 35.1
date: 1995/05/03 23:49:24;  author: jeffm;  state: Exp;
New test - checks page crosser scenarios.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/dcacheharder8.S,v
Working file: verify/toplevel/dcacheharder8.S
head: 35.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
```

```
----------------------------
revision 35.1
date: 1995/05/01 21:50:19;  author: jeffm;  state: Exp;
New test - check gtlb setup where only write access is available, not
read access.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/ex11test4.S,v
Working file: verify/toplevel/ex11test4.S
head: 35.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 6
description:
----------------------------
revision 35.6
date: 1995/05/03 23:37:47;  author: jeffm;  state: Exp;  lines: +22 -1
Fixed FVA's for illegal store size cases. Passes terp (unreleased version
that has support for the new ex11 cases).
----------------------------
revision 35.5
date: 1995/05/03 19:09:22;  author: jeffm;  state: Exp;  lines: +5 -2
Fixed stoooopid code bug.
----------------------------
revision 35.4
date: 1995/05/03 06:10:37;  author: jeffm;  state: Exp;  lines: +7 -17
Exception handler was clobbering register used in result checking.
----------------------------
revision 35.3
date: 1995/05/03 00:53:22;  author: jeffm;  state: Exp;  lines: +3 -2
Access type for synch op exceptions changed to load type.
----------------------------
revision 35.2
date: 1995/05/02 23:24:14;  author: jeffm;  state: Exp;  lines: +3 -3
Result check for case1 was bad.
----------------------------
revision 35.1
date: 1995/05/01 22:57:40;  author: jeffm;  state: Exp;
Test uncached bgate, synch ops, and illegal sizes of uncached stores.
Since terp does not support these exception cases yet, the test
is untested.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/expgcross.S,v
Working file: verify/toplevel/expgcross.S
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/05/04 23:55:03;  author: jeffm;  state: Exp;
```

```
Try to recreate failure seen with nullTest - page cross interfering
with branch target exception handling.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/ife_debug.sig,v
Working file: verify/toplevel/ife_debug.sig
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 35.2
date: 1995/05/03 18:49:56;  author: jeffm;  state: Exp;  lines: +9 -0
Added signals.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/preem_debug.sig,v
Working file: verify/toplevel/preem_debug.sig
head: 35.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 35.2
date: 1995/05/04 21:52:24;  author: jeffm;  state: Exp;  lines: +10 -6
Added more signals - for looking at nullTest.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/trgt_debug.sig,v
Working file: verify/toplevel/trgt_debug.sig
head: 35.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 35.1
date: 1995/05/04 19:32:34;  author: jeffm;  state: Exp;
Trace branch target exception pipe.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/ukernel/BOM,v
Working file: verify/ukernel/BOM
head: 8.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 2
```

```
description:
releasebom adding BOM
----------------------------
revision 6.0
date: 1995/05/03 02:06:33;  author: doi;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/ukernel

name of kernel changed (hwsimkernel instead of kernel.nocalliope) and rules to
make .lst files
----------------------------
revision 5.1
date: 1995/05/03 02:06:23;  author: doi;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/ukernel/Makefile,v
Working file: verify/ukernel/Makefile
head: 1.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 2
description:
----------------------------
revision 1.9
date: 1995/05/03 02:00:58;  author: doi;  state: Exp;  lines: +19 -2
add rules to make .lst files from the stb area (unstripped)
----------------------------
revision 1.8
date: 1995/05/03 00:45:20;  author: doi;  state: Exp;  lines: +2 -2
the name of the kernel (with no calliope) is now hwsimkernel instead of
kernel.nocalliope
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390;  selected revisions: 24
description:
top level verilog BOM
----------------------------
revision 3.548
date: 1995/05/05 04:18:11;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

at/atdisallowxc.pla:
  Target cases were using the gateway permission field instead of the execute
  field.  No cell names changed, so placement still works.
  Test nullTest_pl noticed.  This will probably fix but examination
  of UU exception priorities and preempts is beginning next.
----------------------------
revision 3.547
```

```
date: 1995/05/05 02:40:26;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc


Consolidating recent placement tweaks into .0 BOM.  This version
should place completely at the top level on the first iteration.

Pick up latest top level files:

Makefile.tst
Makefile.vo
genpim2.pl

New drio.power.tab.top in drio section
----------------------------
revision 3.546
date: 1995/05/04 23:11:10;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

fix dc/timing problem with GIhit2CR10_N
----------------------------
revision 3.545
date: 1995/05/04 22:35:10;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

Slight adjustment of placement and power levels to:
1) avoid collisions when u150's on right side power up.
2) reduce absolute sofa clock to output delays.
----------------------------
revision 3.544
date: 1995/05/04 19:29:17;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/au

avoid toplevel collisions
----------------------------
revision 3.543
date: 1995/05/04 17:22:46;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cp

avoid toplevel collisions
----------------------------
revision 3.542
date: 1995/05/04 16:24:51;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

Places rightmost block of flops up against CR and right justifies
so they can grow to the left (u150 cells should grow, they drive
cross-chip wires).
----------------------------
revision 3.541
date: 1995/05/04 07:34:26;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
```

```
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
cj/rsrvd.tst:  AUndx1500 now stops at bit 2.
euterpe.status:  Reduce note on sub-octlet stores not illegal to sys reg only.
  Delete fixed bug on nonblocking illegal loads for sych ops and bgate.
icc/icc.pim.txt:  Move big rstOut flop up to new row borrowed from CJ since
  dickson getting collision with IFe at top level.
----------------------------
revision 3.540
date: 1995/05/04 04:33:34;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/icc

avoid toplevel collisions
----------------------------
revision 3.539
date: 1995/05/04 04:31:39;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

avoid top level collisons and deconjest control stripe
----------------------------
revision 3.538
date: 1995/05/04 04:29:36;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions
----------------------------
revision 3.537
date: 1995/05/04 00:25:56;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/nb

releasing better power.tab.top
----------------------------
revision 3.536
date: 1995/05/03 23:24:52;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

avoid toplevel collisions with mc
----------------------------
revision 3.535
date: 1995/05/03 23:12:04;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

at.V: Inhibited the xcLva freeze on dcacheMiss and on gtlb and tdNdx (CC ndx)
conflicts.

at.pim: updated placement.

dcacheharder_woody_V fabbed.
----------------------------
revision 3.534
date: 1995/05/03 16:54:23;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

New drio placement.  New file drio.nearpads.pim.
----------------------------
revision 3.533
```

```
date: 1995/05/02 22:00:23;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cc

right justify rightmost section of layout
----------------------------
revision 3.532
date: 1995/05/02 03:05:42;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

aviod toplevel collisions with cc
----------------------------
revision 3.531
date: 1995/05/01 22:26:18;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 3.530
date: 1995/05/01 04:02:13;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

at/at.V:
  Forgot to hook up this inside at.V; discovered placement no worse than before.
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
----------------------------
revision 3.529
date: 1995/05/01 03:54:19;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.V at/at.V uu/uu_control.pim:
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
  AT placement not updated but I think it was already not usable.
uu/uumemuv.tdcd:  Comment:  explain why we don't improve the espresso phase.
uu/uumemuv.tdcd:  Only hexlet stores were legal to NB; add octlet stores.
{cj,ife,tst}/*?rst.tst:  CPrdibtreq23 & CPwtibtreq5 were missing.
tst/drvchk.V:  Reg bypassing AUndx around SR pointing at stale name.
tst/job.tst:  Mask & div4 reversed for NB case of AUndx1500cR2.
euterpe.status:  CDIO fixed its write-hi-data-in hold violation a long time ago.
uu/uustepuu.pla:  Lessen confusion in comments on split-write ops (GGFMul/ExtrI)
----------------------------
revision 3.528
date: 1995/04/30 18:02:50;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt


Tau fannout fix.
----------------------------
```

```
revision 3.527
date: 1995/04/30 17:54:23;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

pick up genptab.pl for swing force
----------------------------
revision 3.526
date: 1995/04/30 17:14:19;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/io

turn packing back on for io1
----------------------------
revision 3.525
date: 1995/04/29 23:01:59;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc


Releasing at.V

----------------------------
revision 1.56
date: 1995/04/29 13:35:55 LT;  author: woody;  state: Exp;  lines: +4 -6
Wrong again! access type *is* required in nbHiPri bit. It is needed
to sift out the gtlbHit=X cases, such as SN64WRIQ.
----------------------------
revision 1.55
date: 1995/04/29 13:12:32 LT;  author: woody;  state: Exp;  lines: +6 -2
Fix X problem with nbHiPriR11. When the logic was removed from atprchk
gtlbHit was inadvertantly left off. NrmlMem also was removed from the equation
but that was intentional, see comment in at.V for explanation.
----------------------------
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737;  selected revisions: 31
description:
----------------------------
revision 300.0
date: 1995/05/05 04:17:48;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

at/atdisallowxc.pla:
  Target cases were using the gateway permission field instead of the execute
  field.  No cell names changed, so placement still works.
  Test nullTest_pl noticed.  This will probably fix but examination
  of UU exception priorities and preempts is beginning next.
----------------------------
revision 299.1
date: 1995/05/05 04:17:32;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
```

```
revision 299.0
date: 1995/05/05 02:40:08;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating recent placement tweaks into .0 BOM.  This version
should place completely at the top level on the first iteration.

Pick up latest top level files:

Makefile.tst
Makefile.vo
genpim2.pl

New drio.power.tab.top in drio section
----------------------------
revision 298.6
date: 1995/05/05 02:39:56;  author: tbr;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 298.5
date: 1995/05/04 23:10:56;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

fix dc/timing problem with GIhit2CR10_N
----------------------------
revision 298.4
date: 1995/05/04 22:34:54;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

Slight adjustment of placement and power levels to:
1) avoid collisions when u150's on right side power up.
2) reduce absolute sofa clock to output delays.
----------------------------
revision 298.3
date: 1995/05/04 19:28:59;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/au

avoid toplevel collisions
----------------------------
revision 298.2
date: 1995/05/04 17:22:31;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cp

avoid toplevel collisions
----------------------------
revision 298.1
date: 1995/05/04 16:24:30;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

Places rightmost block of flops up against CR and right justifies
so they can grow to the left (u150 cells should grow, they drive
cross-chip wires).
----------------------------
revision 298.0
date: 1995/05/04 07:34:07;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

```
uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
cj/rsrvd.tst:  AUndx1500 now stops at bit 2.
euterpe.status:  Reduce note on sub-octlet stores not illegal to sys reg only.
  Delete fixed bug on nonblocking illegal loads for sych ops and bgate.
icc/icc.pim.txt:  Move big rstOut flop up to new row borrowed from CJ since
  dickson getting collision with IFe at top level.
----------------------------
revision 297.10
date: 1995/05/04 07:33:53;  author: mws;  state: Exp;  lines: +8 -8
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 297.9
date: 1995/05/04 04:33:17;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/icc

avoid toplevel collisions
----------------------------
revision 297.8
date: 1995/05/04 04:31:25;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/mc

avoid top level collisons and deconjest control stripe
----------------------------
revision 297.7
date: 1995/05/04 04:29:17;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions
----------------------------
revision 297.6
date: 1995/05/04 00:25:32;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/nb

releasing better power.tab.top
----------------------------
revision 297.5
date: 1995/05/03 23:24:34;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/es

avoid toplevel collisions with mc
----------------------------
revision 297.4
date: 1995/05/03 23:11:46;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at

at.V: Inhibited the xcLva freeze on dcacheMiss and on gtlb and tdNdx (CC ndx)
conflicts.

at.pim: updated placement.
```

```
dcacheharder_woody_V fabbed.
----------------------------
revision 297.3
date: 1995/05/03 16:54:03;  author: billz;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/drio

New drio placement.  New file drio.nearpads.pim.
----------------------------
revision 297.2
date: 1995/05/02 22:00:05;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/cc

right justify rightmost section of layout
----------------------------
revision 297.1
date: 1995/05/02 03:05:25;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

aviod toplevel collisions with cc
----------------------------
revision 297.0
date: 1995/05/01 22:25:53;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 296.1
date: 1995/05/01 22:25:35;  author: woody;  state: Exp;  lines: +15 -15
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 296.0
date: 1995/05/01 04:01:51;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

at/at.V:
  Forgot to hook up this inside at.V; discovered placement no worse than before.
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
----------------------------
revision 295.1
date: 1995/05/01 04:01:30;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 295.0
date: 1995/05/01 03:54:01;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.V at/at.V uu/uu_control.pim:
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
```

```
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
  AT placement not updated but I think it was already not usable.
uu/uumemuv.tdcd:  Comment:  explain why we don't improve the espresso phase.
uu/uumemuv.tdcd:  Only hexlet stores were legal to NB; add octlet stores.
{cj,ife,tst}/*?rst.tst:  CPrdibtreq23 & CPwtibtreq5 were missing.
tst/drvchk.V:  Reg bypassing AUndx around SR pointing at stale name.
tst/job.tst:  Mask & div4 reversed for NB case of AUndx1500cR2.
euterpe.status:  CDIO fixed its write-hi-data-in hold violation a long time ago.
uu/uustepuu.pla:  Lessen confusion in comments on split-write ops (GGFMul/ExtrI)
----------------------------
revision 294.4
date: 1995/05/01 03:53:47;  author: mws;  state: Exp;  lines: +8 -8
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 294.3
date: 1995/04/30 18:02:27;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/gt


Tau fannout fix.
----------------------------
revision 294.2
date: 1995/04/30 17:54:04;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

pick up genptab.pl for swing force
----------------------------
revision 294.1
date: 1995/04/30 17:14:02;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/io

turn packing back on for io1
----------------------------
revision 294.0
date: 1995/04/29 23:01:41;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Releasing at.V

----------------------------
revision 1.56
date: 1995/04/29 13:35:55 LT;  author: woody;  state: Exp;  lines: +4 -6
Wrong again! access type *is* required in nbHiPri bit. It is needed
to sift out the gtlbHit=X cases, such as SN64WRIQ.
----------------------------
revision 1.55
date: 1995/04/29 13:12:32 LT;  author: woody;  state: Exp;  lines: +6 -2
Fix X problem with nbHiPriR11. When the logic was removed from atprchk
gtlbHit was inadvertantly left off. NrmlMem also was removed from the equation
but that was intentional, see comment in at.V for explanation.
----------------------------
----------------------------
revision 293.5
date: 1995/04/29 23:01:27;  author: lisar;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile,v
Working file: verilog/bsrc/Makefile
head: 1.255
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 255;   selected revisions: 2
description:
----------------------------
revision 1.240
date: 1995/05/01 21:42:16;  author: lisar;  state: Exp;  lines: +4 -3
 Added cerbrom to simfiles
----------------------------
revision 1.239
date: 1995/04/30 22:38:24;  author: lisar;  state: Exp;  lines: +25 -107
Deleted old zycad rules, added p_
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.share,v
Working file: verilog/bsrc/Makefile.share
head: 1.57
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 57;    selected revisions: 1
description:
----------------------------
revision 1.56
date: 1995/04/29 18:43:05;  author: tbr;  state: Exp;  lines: +2 -2
another fix for power.tab dependencies
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v
Working file: verilog/bsrc/Makefile.tst
head: 40.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;   selected revisions: 4
description:
----------------------------
revision 40.75
date: 1995/05/04 17:36:11;  author: geert;  state: Exp;  lines: +13 -60
Run only 1 iteration at the time ...

Took out some unused hardwired geert_euterpe.* stuff
----------------------------
revision 40.74
date: 1995/04/30 17:33:53;  author: tbr;  state: Exp;  lines: +8 -8
change cp to mv in power.tab.top rule
----------------------------
revision 40.73
date: 1995/04/30 04:01:26;  author: tbr;  state: Exp;  lines: +7 -7
```

```
Make power.tab.top depend on chip_ version
----------------------------
revision 40.72
date: 1995/04/30 00:37:54;  author: tbr;  state: Exp;  lines: +11 -5
correct cvs string for power.tab.top.  Hack for single section version
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.vo,v
Working file: verilog/bsrc/Makefile.vo
head: 27.45
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 45;    selected revisions: 6
description:
----------------------------
revision 27.36
date: 1995/05/05 04:37:34;  author: tbr;  state: Exp;  lines: +2 -2
remove .lis and .com file in local gplace rule in case someone else owns em
----------------------------
revision 27.35
date: 1995/05/04 18:44:15;  author: geert;  state: Exp;  lines: +2 -2
Changed .all to .everything

Geert
----------------------------
revision 27.34
date: 1995/05/04 17:37:23;  author: geert;  state: Exp;  lines: +5 -1
I fixed atypo in the change I made

Geert
----------------------------
revision 27.33
date: 1995/04/30 23:20:27;  author: tbr;  state: Exp;  lines: +2 -2
make exit non zero on -iter1 failure
----------------------------
revision 27.32
date: 1995/04/30 15:42:33;  author: tbr;  state: Exp;  lines: +4 -4
change .all to .everything to avoid rule clash
----------------------------
revision 27.31
date: 1995/04/30 03:57:44;  author: tbr;  state: Exp;  lines: +2 -3
remove forced setting of GARDS_DISPLAY - use commandline
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
Working file: verilog/bsrc/euterpe.V
head: 6.431
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 431;    selected revisions: 3
description:
----------------------------
revision 6.416
```

```
date: 1995/05/04 07:23:32;  author: mws;  state: Exp;  lines: +7 -8
uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
euterpe.status:  Reduce note on sub-octlet stores not illegal to sys reg only.
  Delete fixed bug on nonblocking illegal loads for sych ops and bgate.
----------------------------
revision 6.415
date: 1995/05/01 22:12:35;  author: woody;  state: Exp;  lines: +7 -2
euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 6.414
date: 1995/05/01 03:44:28;  author: mws;  state: Exp;  lines: +8 -6
uu/uu.V euterpe.V at/at.V uu/uu_control.pim euterpe.status:
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
  AT placement not updated but I think it was already not usable.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.status,v
Working file: verilog/bsrc/euterpe.status
head: 24.83
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 83;    selected revisions: 5
description:
----------------------------
revision 24.69
date: 1995/05/04 07:23:38;  author: mws;  state: Exp;  lines: +4 -18
uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
euterpe.status:  Reduce note on sub-octlet stores not illegal to sys reg only.
  Delete fixed bug on nonblocking illegal loads for sych ops and bgate.
----------------------------
revision 24.68
date: 1995/05/01 22:14:56;  author: mws;  state: Exp;  lines: +3 -3
Hot news from vant on topt flops/hrbufs inversion.
----------------------------
revision 24.67
date: 1995/05/01 22:11:45;  author: mws;  state: Exp;  lines: +208 -143
Change asterisk bullets to H, S, V, and M bullets.
```

```
  Reorder/reprioritize many items.  Move most out of "must fix" group;
    add deep coma group.  Put back illegal PA for certain NB ops; pending fix.
  Note better what TOpt can do for tau phase check.
  Rework rules of changing cache size.  Update GGFMul half-complete notes.
  Add software concerns on interrupt lockout by eta beat.
  Clarify have-xcptn-reg-need-CC vs have-CC-need-xcptn-reg livelock rareness.
  Add Craigs rqst for disabling 6 of 8 ICache fill collisions.
  Clean up DTags=X & cache size=0 note and note on br pred must not be xcptn.
  Generally note that ooo jobs should machine check if they get a RAM collision.
  Since we only want bugs here, removed notes
    saying GTLB collision won't upset ooo's,
    that branch prediction won't be fooled into holding xcptn-causing target,
    R1 event entry dependencies need different spacings tested.
----------------------------
revision 24.66
date: 1995/05/01 03:44:23;  author: mws;  state: Exp;  lines: +1 -6
uu/uu.V euterpe.V at/at.V uu/uu_control.pim euterpe.status:
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
  AT placement not updated but I think it was already not usable.
----------------------------
revision 24.65
date: 1995/05/01 03:43:06;  author: mws;  state: Exp;  lines: +14 -2
Clarify icache_except_0 ifetch not getting gtlb etc exceptions bug.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe_wrap.V,v
Working file: verilog/bsrc/euterpe_wrap.V
head: 15.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;   selected revisions: 1
description:
----------------------------
revision 15.93
date: 1995/04/30 22:39:01;  author: lisar;  state: Exp;  lines: +6 -2
Support for p_
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/genpim2.pl,v
Working file: verilog/bsrc/genpim2.pl
head: 41.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 4
description:
----------------------------
revision 41.19
date: 1995/05/04 23:58:04;  author: billz;  state: Exp;  lines: +3 -3
ulow1,2 locations moved slightly to avoid collision with drio cells.
----------------------------
revision 41.18
```

```
date: 1995/05/04 18:40:11;  author: tbr;  state: Exp;  lines: +1 -2
delete obsolete UZCT/U0
----------------------------
revision 41.17
date: 1995/05/03 15:04:07;  author: billz;  state: Exp;  lines: +4 -3
Repositions PADS/ULOW1,2 so they're at the bottom *center*.
Wires are shorter and they don't collide with drio flops.
----------------------------
revision 41.16
date: 1995/05/02 23:30:29;  author: vo;  state: Exp;  lines: +5 -1
moved xb cells from baseplate/custom.pif to here .
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/BOM,v
Working file: verilog/bsrc/at/BOM
head: 93.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 184;   selected revisions: 16
description:
releasebom adding BOM
----------------------------
revision 86.0
date: 1995/05/05 04:11:11;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

at/atdisallowxc.pla:
  Target cases were using the gateway permission field instead of the execute
  field.  No cell names changed, so placement still works.
  Test nullTest_pl noticed.  This will probably fix but examination
  of UU exception priorities and preempts is beginning next.
----------------------------
revision 85.1
date: 1995/05/05 04:11:02;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 85.0
date: 1995/05/04 23:10:40;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/at

fix dc/timing problem with GIhit2CR10_N
----------------------------
revision 84.1
date: 1995/05/04 23:10:33;  author: dickson;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 84.0
date: 1995/05/04 07:27:32;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
```

```
  Found by inspection (thanks woody), seems no test coverage.
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
cj/rsrvd.tst:  AUndx1500 now stops at bit 2.
euterpe.status:  Reduce note on sub-octlet stores not illegal to sys reg only.
  Delete fixed bug on nonblocking illegal loads for sych ops and bgate.
icc/icc.pim.txt:  Move big rstOut flop up to new row borrowed from CJ since
  dickson getting collision with IFe at top level.
----------------------------
revision 83.1
date: 1995/05/04 07:27:25;  author: mws;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 83.0
date: 1995/05/03 23:11:28;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/at

at.V: Inhibited the xcLva freeze on dcacheMiss and on gtlb and tdNdx (CC ndx)
conflicts.

at.pim: updated placement.

dcacheharder_woody_V fabbed.
----------------------------
revision 82.1
date: 1995/05/03 23:11:20;  author: woody;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 82.0
date: 1995/05/01 22:17:24;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 81.1
date: 1995/05/01 22:17:17;  author: woody;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 81.0
date: 1995/05/01 03:56:06;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

at/at.V:
  Forgot to hook up this inside at.V; discovered placement no worse than before.
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
----------------------------
revision 80.1
date: 1995/05/01 03:55:59;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
```

```
revision 80.0
date: 1995/05/01 03:48:03;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.V at/at.V uu/uu_control.pim:
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
  AT placement not updated but I think it was already not usable.
uu/uumemuv.tdcd:  Comment:  explain why we don't improve the espresso phase.
uu/uumemuv.tdcd:  Only hexlet stores were legal to NB; add octlet stores.
{cj,ife,tst}/*?rst.tst:  CPrdibtreq23 & CPwtibtreq5 were missing.
tst/drvchk.V:  Reg bypassing AUndx around SR pointing at stale name.
tst/job.tst:  Mask & div4 reversed for NB case of AUndx1500cR2.
euterpe.status:  CDIO fixed its write-hi-data-in hold violation a long time ago.
uu/uustepuu.pla:  Lessen confusion in comments on split-write ops (GGFMul/ExtrI)
----------------------------
revision 79.1
date: 1995/05/01 03:47:55;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 79.0
date: 1995/04/29 22:56:25;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Releasing at.V

----------------------------
revision 1.56
date: 1995/04/29 13:35:55 LT;  author: woody;  state: Exp;  lines: +4 -6
Wrong again! access type *is* required in nbHiPri bit. It is needed
to sift out the gtlbHit=X cases, such as SN64WRIQ.
----------------------------
revision 1.55
date: 1995/04/29 13:12:32 LT;  author: woody;  state: Exp;  lines: +6 -2
Fix X problem with nbHiPriR11. When the logic was removed from atprchk
gtlbHit was inadvertantly left off. NrmlMem also was removed from the equation
but that was intentional, see comment in at.V for explanation.
----------------------------
----------------------------
revision 78.1
date: 1995/04/29 22:56:18;  author: lisar;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/at.V,v
Working file: verilog/bsrc/at/at.V
head: 1.66
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 66;    selected revisions: 7
description:
----------------------------
revision 1.61
```

```
date: 1995/05/04 07:24:32;  author: mws;  state: Exp;  lines: +17 -17
uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
----------------------------
revision 1.60
date: 1995/05/03 23:09:43;  author: woody;  state: Exp;  lines: +30 -10
at.V: Inhibited the xcLva freeze on dcacheMiss and on gtlb and tdNdx (CC ndx)
conflicts.

at.pim: updated placement.

dcacheharder_woody_V fabbed.
----------------------------
revision 1.59
date: 1995/05/01 22:13:59;  author: woody;  state: Exp;  lines: +14 -9
euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 1.58
date: 1995/05/01 03:54:46;  author: mws;  state: Exp;  lines: +2 -2
didn't hook up last change right
----------------------------
revision 1.57
date: 1995/05/01 03:46:53;  author: mws;  state: Exp;  lines: +4 -2
uu/uu.V euterpe.V at/at.V uu/uu_control.pim:
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
  AT placement not updated but I think it was already not usable.
----------------------------
revision 1.56
date: 1995/04/29 20:35:55;  author: woody;  state: Exp;  lines: +4 -6
Wrong again! access type *is* required in nbHiPri bit. It is needed
to sift out the gtlbHit=X cases, such as SN64WRIQ.
----------------------------
revision 1.55
date: 1995/04/29 20:12:32;  author: woody;  state: Exp;  lines: +6 -2
Fix X problem with nbHiPriR11. When the logic was removed from atprchk
gtlbHit was inadvertantly left off. NrmlMem also was removed from the equation
but that was intentional, see comment in at.V for explanation.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/at.pim,v
Working file: verilog/bsrc/at/at.pim
head: 51.23
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 23;    selected revisions: 5
description:
----------------------------
revision 51.21
date: 1995/05/04 23:09:49;  author: dickson;  state: Exp;  lines: +119 -136
fix dc load and timing problem with GIhit2CR10_N
----------------------------
revision 51.20
date: 1995/05/04 07:24:37;  author: mws;  state: Exp;  lines: +5 -2
uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
----------------------------
revision 51.19
date: 1995/05/03 23:09:48;  author: woody;  state: Exp;  lines: +2 -0
at.V: Inhibited the xcLva freeze on dcacheMiss and on gtlb and tdNdx (CC ndx)
conflicts.

at.pim: updated placement.

dcacheharder_woody_V fabbed.
----------------------------
revision 51.18
date: 1995/05/01 22:14:02;  author: woody;  state: Exp;  lines: +513 -507
euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 51.17
date: 1995/05/01 18:07:42;  author: woody;  state: Exp;  lines: +3 -1
check in intermediate results.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/atdisallowxc.pla,v
Working file: verilog/bsrc/at/atdisallowxc.pla
head: 1.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 1.5
date: 1995/05/05 04:02:16;  author: mws;  state: Exp;  lines: +13 -13
at/atdisallowxc.pla:
  Target cases were using the gateway permission field instead of the execute
  field.  No cell names changed, so placement still works.
  Test nullTest_pl noticed.  This will probably fix but examination
```

```
  of UU exception priorities and preempts is beginning next.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/atnbreq.Veqn,v
Working file: verilog/bsrc/at/atnbreq.Veqn
head: 2.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 2.4
date: 1995/05/01 22:14:05;  author: woody;  state: Exp;  lines: +4 -4
euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/atpadcd.Veqn,v
Working file: verilog/bsrc/at/atpadcd.Veqn
head: 1.25
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 25;    selected revisions: 1
description:
----------------------------
revision 1.24
date: 1995/05/01 22:14:07;  author: woody;  state: Exp;  lines: +18 -7
euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/atxcfrz.Veqn,v
Working file: verilog/bsrc/at/atxcfrz.Veqn
head: 1.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 1.2
date: 1995/05/04 07:24:41;  author: mws;  state: Exp;  lines: +10 -5
```

```
uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/clean-request,v
Working file: verilog/bsrc/at/clean-request
head: 4.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 4.11
date: 1995/05/04 23:09:51;  author: dickson;  state: Exp;  lines: +1 -0
fix dc load and timing problem with GIhit2CR10_N
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/BOM,v
Working file: verilog/bsrc/au/BOM
head: 44.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 89;    selected revisions: 2
description:
----------------------------
revision 41.0
date: 1995/05/04 19:28:36;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/au

avoid toplevel collisions
----------------------------
revision 40.1
date: 1995/05/04 19:28:29;  author: dickson;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/auindx.pim,v
Working file: verilog/bsrc/au/auindx.pim
head: 12.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 12.10
date: 1995/05/04 19:27:50;  author: dickson;  state: Exp;  lines: +87 -115
avoid top-level collisions
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/au/clean-request,v
Working file: verilog/bsrc/au/clean-request
head: 14.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 14.8
date: 1995/05/04 19:27:52;  author: dickson;  state: Exp;  lines: +2 -1
avoid top-level collisions
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/BOM,v
Working file: verilog/bsrc/cc/BOM
head: 92.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 84.0
date: 1995/05/02 21:59:45;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/cc

right justify rightmost section of layout
----------------------------
revision 83.1
date: 1995/05/02 21:59:38;  author: dickson;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 83.0
date: 1995/05/01 22:17:57;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 82.1
date: 1995/05/01 22:17:50;  author: woody;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc.V,v
Working file: verilog/bsrc/cc/cc.V
```

```
head: 1.87
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 87;    selected revisions: 1
description:
----------------------------
revision 1.81
date: 1995/05/01 22:14:27;  author: woody;  state: Exp;  lines: +4 -4
euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/cc.power.tab.top,v
Working file: verilog/bsrc/cc/cc.power.tab.top
head: 32.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 32.7
date: 1995/04/29 20:26:30;  author: tbr;  state: Exp;  lines: +1059 -13
correct vref swings
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/ccstart.Veqn,v
Working file: verilog/bsrc/cc/ccstart.Veqn
head: 24.18
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 18;    selected revisions: 1
description:
----------------------------
revision 24.18
date: 1995/05/01 22:14:30;  author: woody;  state: Exp;  lines: +4 -4
euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/ccstart_custom.pim,v
Working file: verilog/bsrc/cc/ccstart_custom.pim
```

```
head: 77.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 77.2
date: 1995/05/01 22:14:31;  author: woody;  state: Exp;  lines: +2 -1
euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/clean-request,v
Working file: verilog/bsrc/cc/clean-request
head: 14.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
----------------------------
revision 14.13
date: 1995/05/02 21:58:37;  author: dickson;  state: Exp;  lines: +1 -0
right justify right most section
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cc/genpim.pl,v
Working file: verilog/bsrc/cc/genpim.pl
head: 5.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
----------------------------
revision 5.20
date: 1995/05/02 21:58:39;  author: dickson;  state: Exp;  lines: +3 -2
right justify right most section
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/BOM,v
Working file: verilog/bsrc/cdio/BOM
head: 55.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 110;   selected revisions: 2
```

```
description:
releasebom adding BOM
----------------------------
revision 52.0
date: 1995/05/01 22:18:22;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 51.1
date: 1995/05/01 22:18:14;  author: woody;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cdio/cdio.power.tab.top,v
Working file: verilog/bsrc/cdio/cdio.power.tab.top
head: 34.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 34.10
date: 1995/04/29 20:26:35;  author: tbr;  state: Exp;  lines: +34 -32
correct vref swings
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/BOM,v
Working file: verilog/bsrc/cj/BOM
head: 122.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 259;   selected revisions: 4
description:
----------------------------
revision 118.0
date: 1995/05/04 07:28:26;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
cj/rsrvd.tst:  AUndx1500 now stops at bit 2.
```

```
euterpe.status:  Reduce note on sub-octlet stores not illegal to sys reg only.
  Delete fixed bug on nonblocking illegal loads for sych ops and bgate.
icc/icc.pim.txt:  Move big rstOut flop up to new row borrowed from CJ since
  dickson getting collision with IFe at top level.
----------------------------
revision 117.1
date: 1995/05/04 07:28:18;  author: mws;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 117.0
date: 1995/05/01 03:48:57;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.V at/at.V uu/uu_control.pim:
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
  AT placement not updated but I think it was already not usable.
uu/uumemuv.tdcd:  Comment:  explain why we don't improve the espresso phase.
uu/uumemuv.tdcd:  Only hexlet stores were legal to NB; add octlet stores.
{cj,ife,tst}/*?rst.tst:  CPrdibtreq23 & CPwtibtreq5 were missing.
tst/drvchk.V:  Reg bypassing AUndx around SR pointing at stale name.
tst/job.tst:  Mask & div4 reversed for NB case of AUndx1500cR2.
euterpe.status:  CDIO fixed its write-hi-data-in hold violation a long time ago.
uu/uustepuu.pla:  Lessen confusion in comments on split-write ops (GGFMul/ExtrI)
----------------------------
revision 116.1
date: 1995/05/01 03:48:50;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/cjrst.tst,v
Working file: verilog/bsrc/cj/cjrst.tst
head: 13.39
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 39;    selected revisions: 2
description:
----------------------------
revision 13.38
date: 1995/05/04 07:26:03;  author: mws;  state: Exp;  lines: +2 -2
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
cj/rsrvd.tst:  AUndx1500 now stops at bit 2.
----------------------------
revision 13.37
date: 1995/05/01 03:35:52;  author: mws;  state: Exp;  lines: +3 -2
{cj,ife,tst}/*?rst.tst:  CPrdibtreq23 & CPwtibtreq5 were missing.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/rsrvd.tst,v
Working file: verilog/bsrc/cj/rsrvd.tst
head: 78.13
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
----------------------------
revision 78.11
date: 1995/05/04 07:26:05;  author: mws;  state: Exp;  lines: +3 -3
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
cj/rsrvd.tst:  AUndx1500 now stops at bit 2.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/BOM,v
Working file: verilog/bsrc/cp/BOM
head: 60.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 119;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 55.0
date: 1995/05/04 17:22:15;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/cp

avoid toplevel collisions
----------------------------
revision 54.1
date: 1995/05/04 17:22:08;  author: dickson;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/clean-request,v
Working file: verilog/bsrc/cp/clean-request
head: 9.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 9.9
date: 1995/05/04 17:20:38;  author: dickson;  state: Exp;  lines: +2 -1
avoid collisions at toplevel
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cph.pim,v
Working file: verilog/bsrc/cp/cph.pim
head: 41.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
```

```
revision 41.7
date: 1995/05/04 17:20:40;  author: dickson;  state: Exp;  lines: +274 -275
avoid collisions at toplevel
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/cphh.pim,v
Working file: verilog/bsrc/cp/cphh.pim
head: 47.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 47.2
date: 1995/05/04 17:20:41;  author: dickson;  state: Exp;  lines: +238 -238
avoid collisions at toplevel
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cp/genpim.pl,v
Working file: verilog/bsrc/cp/genpim.pl
head: 5.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 5.11
date: 1995/05/04 17:20:43;  author: dickson;  state: Exp;  lines: +2 -2
avoid collisions at toplevel
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/drio/BOM,v
Working file: verilog/bsrc/drio/BOM
head: 26.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 50;    selected revisions: 8
description:
releasebom adding BOM
----------------------------
revision 24.0
date: 1995/05/05 02:36:08;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Consolidating recent placement tweaks into .0 BOM.  This version
should place completely at the top level on the first iteration.

Pick up latest top level files:

Makefile.tst
```

```
Makefile.vo
genpim2.pl

New drio.power.tab.top in drio section
----------------------------
revision 23.1
date: 1995/05/05 02:36:01;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 23.0
date: 1995/05/04 22:34:39;  author: billz;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/drio

Slight adjustment of placement and power levels to:
1) avoid collisions when u150's on right side power up.
2) reduce absolute sofa clock to output delays.
----------------------------
revision 22.1
date: 1995/05/04 22:34:33;  author: billz;  state: Exp;  lines: +3 -5
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 22.0
date: 1995/05/04 16:24:10;  author: billz;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/drio

Places rightmost block of flops up against CR and right justifies
so they can grow to the left (u150 cells should grow, they drive
cross-chip wires).
----------------------------
revision 21.1
date: 1995/05/04 16:24:03;  author: billz;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 21.0
date: 1995/05/03 16:53:43;  author: billz;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/drio

New drio placement.  New file drio.nearpads.pim.
----------------------------
revision 20.1
date: 1995/05/03 16:53:35;  author: billz;  state: Exp;  lines: +6 -5
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/drio/Makefile,v
Working file: verilog/bsrc/drio/Makefile
head: 1.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 1.5
date: 1995/05/03 14:53:06;  author: billz;  state: Exp;  lines: +3 -1
New drio placement. Flops near appropriate pad drivers.
```

```
Note u100,110,130,140 -- primary outputs -- are 2s sized in power.tab.local.
u120 -- primary output with x8 the load -- 16s, sized in power.tab.local.
u150 are outputs which go to dr and must be sized by topt.  Generally
ones on right drive wires which traverse chip and will be bigger than
those on left.
Note also this placement depends on correct c01 cell (found in "euterpe_pads"
and placed in ../genpim2.pl) placement.  These cells drive ttle2eu enables
for those outputs which are never tri-stated.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/drio/drio.nearpads.pim,v
Working file: verilog/bsrc/drio/drio.nearpads.pim
head: 20.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 3
description:
----------------------------
revision 20.3
date: 1995/05/04 22:33:42;  author: billz;  state: Exp;  lines: +7 -2
Slight adjustment of placement and power levels to:
1) avoid collisions when u150's on right side power up.
2) reduce absolute sofa clock to output delays.

Removed defunct files.
----------------------------
revision 20.2
date: 1995/05/03 22:53:22;  author: billz;  state: Exp;  lines: +4 -2
Places rightmost block of flops up against CR and right justifies
so they can grow to the left (u150 cells should grow, they drive
cross-chip wires).
----------------------------
revision 20.1
date: 1995/05/03 14:53:08;  author: billz;  state: Exp;
New drio placement. Flops near appropriate pad drivers.
Note u100,110,130,140 -- primary outputs -- are 2s sized in power.tab.local.
u120 -- primary output with x8 the load -- 16s, sized in power.tab.local.
u150 are outputs which go to dr and must be sized by topt.  Generally
ones on right drive wires which traverse chip and will be bigger than
those on left.
Note also this placement depends on correct c01 cell (found in "euterpe_pads"
and placed in ../genpim2.pl) placement.  These cells drive ttle2eu enables
for those outputs which are never tri-stated.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/drio/drio.power.tab.top,v
Working file: verilog/bsrc/drio/drio.power.tab.top
head: 9.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 2
description:
----------------------------
```

```
revision 9.10
date: 1995/05/05 01:35:57;  author: tbr;  state: Exp;  lines: +144 -28
update power.tab.top from latest top level
----------------------------
revision 9.9
date: 1995/05/03 14:53:09;  author: billz;  state: Exp;  lines: +0 -116
New drio placement. Flops near appropriate pad drivers.
Note u100,110,130,140 -- primary outputs -- are 2s sized in power.tab.local.
u120 -- primary output with x8 the load -- 16s, sized in power.tab.local.
u150 are outputs which go to dr and must be sized by topt.  Generally
ones on right drive wires which traverse chip and will be bigger than
those on left.
Note also this placement depends on correct c01 cell (found in "euterpe_pads"
and placed in ../genpim2.pl) placement.  These cells drive ttle2eu enables
for those outputs which are never tri-stated.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/drio/genpim.pl,v
Working file: verilog/bsrc/drio/genpim.pl
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 1.4
date: 1995/05/03 14:53:10;  author: billz;  state: Exp;  lines: +3 -15
New drio placement. Flops near appropriate pad drivers.
Note u100,110,130,140 -- primary outputs -- are 2s sized in power.tab.local.
u120 -- primary output with x8 the load -- 16s, sized in power.tab.local.
u150 are outputs which go to dr and must be sized by topt.  Generally
ones on right drive wires which traverse chip and will be bigger than
those on left.
Note also this placement depends on correct c01 cell (found in "euterpe_pads"
and placed in ../genpim2.pl) placement.  These cells drive ttle2eu enables
for those outputs which are never tri-stated.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/drio/power.tab.local,v
Working file: verilog/bsrc/drio/power.tab.local
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 2
description:
----------------------------
revision 1.3
date: 1995/05/04 22:33:44;  author: billz;  state: Exp;  lines: +55 -55
Slight adjustment of placement and power levels to:
1) avoid collisions when u150's on right side power up.
2) reduce absolute sofa clock to output delays.

Removed defunct files.
```

```
----------------------------
revision 1.2
date: 1995/05/03 14:53:11;  author: billz;  state: Exp;  lines: +59 -57
New drio placement. Flops near appropriate pad drivers.
Note u100,110,130,140 -- primary outputs -- are 2s sized in power.tab.local.
u120 -- primary output with x8 the load -- 16s, sized in power.tab.local.
u150 are outputs which go to dr and must be sized by topt.  Generally
ones on right drive wires which traverse chip and will be bigger than
those on left.
Note also this placement depends on correct c01 cell (found in "euterpe_pads"
and placed in ../genpim2.pl) placement.  These cells drive ttle2eu enables
for those outputs which are never tri-stated.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/BOM,v
Working file: verilog/bsrc/es/BOM
head: 97.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 198;   selected revisions: 2
description:
----------------------------
revision 90.0
date: 1995/05/03 23:24:14;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/es

avoid toplevel collisions with mc
----------------------------
revision 89.1
date: 1995/05/03 23:24:06;  author: dickson;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/es/es.pim,v
Working file: verilog/bsrc/es/es.pim
head: 5.55
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 55;    selected revisions: 1
description:
----------------------------
revision 5.50
date: 1995/05/03 21:37:43;  author: dickson;  state: Exp;  lines: +520 -520
placement change to eliminate collisons with mc at toplevel
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/gt/BOM,v
Working file: verilog/bsrc/gt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 194;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 92.0
date: 1995/04/30 18:02:03;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/gt


Tau fannout fix.
----------------------------
revision 91.1
date: 1995/04/30 18:01:53;  author: tbr;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 91.0
date: 1995/04/29 22:58:28;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Releasing at.V

----------------------------
revision 1.56
date: 1995/04/29 13:35:55 LT;  author: woody;  state: Exp;  lines: +4 -6
Wrong again! access type *is* required in nbHiPri bit. It is needed
to sift out the gtlbHit=X cases, such as SN64WRIQ.
----------------------------
revision 1.55
date: 1995/04/29 13:12:32 LT;  author: woody;  state: Exp;  lines: +6 -2
Fix X problem with nbHiPriR11. When the logic was removed from atprchk
gtlbHit was inadvertantly left off. NrmlMem also was removed from the equation
but that was intentional, see comment in at.V for explanation.
----------------------------
----------------------------
revision 90.1
date: 1995/04/29 22:58:21;  author: lisar;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/BOM,v
Working file: verilog/bsrc/icc/BOM
head: 49.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 96;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 45.0
date: 1995/05/04 04:32:58;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/icc

avoid toplevel collisions
----------------------------
```

```
revision 44.1
date: 1995/05/04 04:32:51;  author: dickson;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/icc/icc.pim.txt,v
Working file: verilog/bsrc/icc/icc.pim.txt
head: 39.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 39.4
date: 1995/05/03 23:11:52;  author: mws;  state: Exp;  lines: +2 -1
Move big rstOut flop up to new row borrowed from CJ since
  dickson getting collision with IFe at top level.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/BOM,v
Working file: verilog/bsrc/ife/BOM
head: 68.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 140;   selected revisions: 2
description:
----------------------------
revision 67.0
date: 1995/05/01 03:50:55;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.V at/at.V uu/uu_control.pim:
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
  AT placement not updated but I think it was already not usable.
uu/uumemuv.tdcd:  Comment:  explain why we don't improve the espresso phase.
uu/uumemuv.tdcd:  Only hexlet stores were legal to NB; add octlet stores.
{cj,ife,tst}/*?rst.tst:  CPrdibtreq23 & CPwtibtreq5 were missing.
tst/drvchk.V:  Reg bypassing AUndx around SR pointing at stale name.
tst/job.tst:  Mask & div4 reversed for NB case of AUndx1500cR2.
euterpe.status:  CDIO fixed its write-hi-data-in hold violation a long time ago.
uu/uustepuu.pla:  Lessen confusion in comments on split-write ops (GGFMul/ExtrI)
----------------------------
revision 66.1
date: 1995/05/01 03:50:48;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ife/ifrst.tst,v
Working file: verilog/bsrc/ife/ifrst.tst
head: 2.12
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 2.12
date: 1995/05/01 03:38:18;  author: mws;  state: Exp;  lines: +2 -2
{cj,ife,tst}/*?rst.tst:  CPrdibtreq23 & CPwtibtreq5 were missing.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/BOM,v
Working file: verilog/bsrc/io/BOM
head: 48.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 94;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 44.0
date: 1995/04/30 17:13:44;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/io

turn packing back on for io1
----------------------------
revision 43.1
date: 1995/04/30 17:13:38;  author: tbr;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/Makefile,v
Working file: verilog/bsrc/io/Makefile
head: 1.18
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 18;    selected revisions: 1
description:
----------------------------
revision 1.17
date: 1995/04/30 17:13:15;  author: tbr;  state: Exp;  lines: +1 -3
turn packing back on for io1
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/io/pimlib.pl,v
Working file: verilog/bsrc/io/pimlib.pl
head: 4.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
```

```
----------------------------
revision 4.9
date: 1995/04/30 17:13:17;  author: tbr;  state: Exp;  lines: +17 -6
turn packing back on for io1
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/BOM,v
Working file: verilog/bsrc/lt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 196;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 94.0
date: 1995/05/01 22:21:46;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 93.1
date: 1995/05/01 22:21:38;  author: woody;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/lt.power.tab.top,v
Working file: verilog/bsrc/lt/lt.power.tab.top
head: 68.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 68.12
date: 1995/04/29 20:26:27;  author: tbr;  state: Exp;  lines: +2 -0
correct vref swings
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/BOM,v
Working file: verilog/bsrc/mc/BOM
head: 79.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 157;   selected revisions: 4
```

```
description:
releasebom adding BOM
----------------------------
revision 72.0
date: 1995/05/04 04:31:09;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/mc

avoid top level collisons and deconjest control stripe
----------------------------
revision 71.1
date: 1995/05/04 04:31:02;  author: dickson;  state: Exp;  lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 71.0
date: 1995/05/01 22:22:10;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 70.1
date: 1995/05/01 22:22:03;  author: woody;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/clean-request,v
Working file: verilog/bsrc/mc/clean-request
head: 17.19
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 19;    selected revisions: 1
description:
----------------------------
revision 17.17
date: 1995/05/04 04:29:52;  author: dickson;  state: Exp;  lines: +2 -1
avoid toplevel collisions.
tried to free up routing chanels in control stripe.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc.control.pim,v
Working file: verilog/bsrc/mc/mc.control.pim
head: 48.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 48.7
```

```
date: 1995/05/04 04:29:54;  author: dickson;  state: Exp;  lines: +572 -572
avoid toplevel collisions.
tried to free up routing chanels in control stripe.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc.dataHigh.pim,v
Working file: verilog/bsrc/mc/mc.dataHigh.pim
head: 48.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 48.7
date: 1995/05/04 04:29:56;  author: dickson;  state: Exp;  lines: +1300 -1268
avoid toplevel collisions.
tried to free up routing chanels in control stripe.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc.dataLow.pim,v
Working file: verilog/bsrc/mc/mc.dataLow.pim
head: 48.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 48.6
date: 1995/05/04 04:29:59;  author: dickson;  state: Exp;  lines: +32 -0
avoid toplevel collisions.
tried to free up routing chanels in control stripe.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc.power.tab.top,v
Working file: verilog/bsrc/mc/mc.power.tab.top
head: 37.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 37.10
date: 1995/04/29 20:26:19;  author: tbr;  state: Exp;  lines: +275 -275
correct vref swings
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/mc/mc_xlud.V,v
Working file: verilog/bsrc/mc/mc_xlud.V
head: 28.4
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 28.4
date: 1995/05/04 04:30:01;  author: dickson;  state: Exp;  lines: +6 -4
avoid toplevel collisions.
tried to free up routing chanels in control stripe.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/BOM,v
Working file: verilog/bsrc/nb/BOM
head: 130.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 261;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 126.0
date: 1995/05/04 00:25:07;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/nb

releasing better power.tab.top
----------------------------
revision 125.1
date: 1995/05/04 00:24:57;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 125.0
date: 1995/05/01 22:23:00;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 124.1
date: 1995/05/01 22:22:51;  author: woody;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/nb/nb.power.tab.top,v
Working file: verilog/bsrc/nb/nb.power.tab.top
head: 82.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 3
```

```
description:
----------------------------
revision 82.12
date: 1995/05/02 00:18:50;  author: tbr;  state: Exp;  lines: +710 -710
regenerated with dccheckonly for vref generator
----------------------------
revision 82.11
date: 1995/04/30 00:36:46;  author: tbr;  state: Exp;  lines: +1 -1
try to fix cvs string
----------------------------
revision 82.10
date: 1995/04/29 20:26:01;  author: tbr;  state: Exp;  lines: +630 -628
correct vref swings
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/BOM,v
Working file: verilog/bsrc/rg/BOM
head: 136.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 297;   selected revisions: 4
description:
----------------------------
revision 124.0
date: 1995/05/04 07:31:51;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
cj/rsrvd.tst:  AUndx1500 now stops at bit 2.
euterpe.status:  Reduce note on sub-octlet stores not illegal to sys reg only.
  Delete fixed bug on nonblocking illegal loads for sych ops and bgate.
icc/icc.pim.txt:  Move big rstOut flop up to new row borrowed from CJ since
  dickson getting collision with IFe at top level.
----------------------------
revision 123.1
date: 1995/05/04 07:31:43;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 123.0
date: 1995/05/04 04:28:56;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/rg

avoid toplevel collisions
----------------------------
revision 122.1
date: 1995/05/04 04:28:48;  author: dickson;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/clean-request,v
Working file: verilog/bsrc/rg/clean-request
head: 60.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 60.11
date: 1995/05/04 04:27:55;  author: dickson;  state: Exp;  lines: +1 -0
avoid toplevel collisions
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rg.pim,v
Working file: verilog/bsrc/rg/rg.pim
head: 82.31
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 31;    selected revisions: 1
description:
----------------------------
revision 82.22
date: 1995/05/04 04:27:59;  author: dickson;  state: Exp;  lines: +950 -999
avoid toplevel collisions
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/rg/rgrst.tst,v
Working file: verilog/bsrc/rg/rgrst.tst
head: 9.28
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28;    selected revisions: 1
description:
----------------------------
revision 9.28
date: 1995/05/04 07:25:31;  author: mws;  state: Exp;  lines: +2 -2
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/BOM,v
Working file: verilog/bsrc/sr/BOM
head: 75.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;   selected revisions: 6
description:
releasebom adding BOM
----------------------------
revision 70.0
```

```
date: 1995/05/02 03:05:08;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/sr

aviod toplevel collisions with cc
----------------------------
revision 69.1
date: 1995/05/02 03:05:01;  author: dickson;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 69.0
date: 1995/04/30 17:53:44;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/sr

pick up genptab.pl for swing force
----------------------------
revision 68.1
date: 1995/04/30 17:53:37;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 68.0
date: 1995/04/29 23:00:25;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc


Releasing at.V

----------------------------
revision 1.56
date: 1995/04/29 13:35:55 LT;  author: woody;  state: Exp;  lines: +4 -6
Wrong again! access type *is* required in nbHiPri bit. It is needed
to sift out the gtlbHit=X cases, such as SN64WRIQ.
----------------------------
revision 1.55
date: 1995/04/29 13:12:32 LT;  author: woody;  state: Exp;  lines: +6 -2
Fix X problem with nbHiPriR11. When the logic was removed from atprchk
gtlbHit was inadvertantly left off. NrmlMem also was removed from the equation
but that was intentional, see comment in at.V for explanation.
----------------------------
----------------------------
revision 67.1
date: 1995/04/29 23:00:18;  author: lisar;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/clean-request,v
Working file: verilog/bsrc/sr/clean-request
head: 26.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 26.11
date: 1995/05/02 03:04:10;  author: dickson;  state: Exp;  lines: +2 -1
avoid toplevel collisions with cc
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/sr.pim,v
Working file: verilog/bsrc/sr/sr.pim
head: 51.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 1
description:
----------------------------
revision 51.10
date: 1995/05/02 03:04:12;  author: dickson;  state: Exp;  lines: +1665 -1665
avoid toplevel collisions with cc
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/BOM,v
Working file: verilog/bsrc/tst/BOM
head: 112.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 234;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 110.0
date: 1995/05/04 07:32:26;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
cj/rsrvd.tst:  AUndx1500 now stops at bit 2.
euterpe.status:  Reduce note on sub-octlet stores not illegal to sys reg only.
  Delete fixed bug on nonblocking illegal loads for sych ops and bgate.
icc/icc.pim.txt:  Move big rstOut flop up to new row borrowed from CJ since
  dickson getting collision with IFe at top level.
----------------------------
revision 109.1
date: 1995/05/04 07:32:18;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 109.0
date: 1995/05/01 03:52:31;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.V at/at.V uu/uu_control.pim:
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
```

```
  AT placement not updated but I think it was already not usable.
uu/uumemuv.tdcd:  Comment:  explain why we don't improve the espresso phase.
uu/uumemuv.tdcd:  Only hexlet stores were legal to NB; add octlet stores.
{cj,ife,tst}/*?rst.tst:  CPrdibtreq23 & CPwtibtreq5 were missing.
tst/drvchk.V:  Reg bypassing AUndx around SR pointing at stale name.
tst/job.tst:  Mask & div4 reversed for NB case of AUndx1500cR2.
euterpe.status:  CDIO fixed its write-hi-data-in hold violation a long time ago.
uu/uustepuu.pla:  Lessen confusion in comments on split-write ops (GGFMul/ExtrI)
----------------------------
revision 108.1
date: 1995/05/01 03:52:23;  author: mws;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/drvchk.V,v
Working file: verilog/bsrc/tst/drvchk.V
head: 1.85
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 85;    selected revisions: 2
description:
----------------------------
revision 1.83
date: 1995/05/04 07:26:20;  author: mws;  state: Exp;  lines: +3 -1
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
----------------------------
revision 1.82
date: 1995/05/01 03:41:14;  author: mws;  state: Exp;  lines: +2 -2
{cj,ife,tst}/*?rst.tst:  CPrdibtreq23 & CPwtibtreq5 were missing.
tst/drvchk.V:  Reg bypassing AUndx around SR pointing at stale name.
tst/job.tst:  Mask & div4 reversed for NB case of AUndx1500cR2.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/job.tst,v
Working file: verilog/bsrc/tst/job.tst
head: 6.41
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 41;    selected revisions: 1
description:
----------------------------
revision 6.40
date: 1995/05/01 03:41:17;  author: mws;  state: Exp;  lines: +2 -2
{cj,ife,tst}/*?rst.tst:  CPrdibtreq23 & CPwtibtreq5 were missing.
tst/drvchk.V:  Reg bypassing AUndx around SR pointing at stale name.
tst/job.tst:  Mask & div4 reversed for NB case of AUndx1500cR2.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/tst/tstrst.tst,v
Working file: verilog/bsrc/tst/tstrst.tst
head: 6.35
branch:
locks: strict
```

```
access list:
keyword substitution: kv
total revisions: 35;    selected revisions: 1
description:
----------------------------
revision 6.35
date: 1995/05/01 03:41:19;  author: mws;  state: Exp;  lines: +2 -2
{cj,ife,tst}/*?rst.tst:  CPrdibtreq23 & CPwtibtreq5 were missing.
tst/drvchk.V:  Reg bypassing AUndx around SR pointing at stale name.
tst/job.tst:  Mask & div4 reversed for NB case of AUndx1500cR2.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v
Working file: verilog/bsrc/uu/BOM
head: 218.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 480;   selected revisions: 6
description:
----------------------------
revision 194.0
date: 1995/05/04 07:32:59;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
cj/rsrvd.tst:  AUndx1500 now stops at bit 2.
euterpe.status:  Reduce note on sub-octlet stores not illegal to sys reg only.
  Delete fixed bug on nonblocking illegal loads for sych ops and bgate.
icc/icc.pim.txt:  Move big rstOut flop up to new row borrowed from CJ since
  dickson getting collision with IFe at top level.
----------------------------
revision 193.1
date: 1995/05/04 07:32:50;  author: mws;  state: Exp;  lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 193.0
date: 1995/05/01 22:24:28;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 192.1
date: 1995/05/01 22:24:18;  author: woody;  state: Exp;  lines: +3 -3
```

```
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 192.0
date: 1995/05/01 03:53:00;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.V at/at.V uu/uu_control.pim:
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
  AT placement not updated but I think it was already not usable.
uu/uumemuv.tdcd:  Comment:  explain why we don't improve the espresso phase.
uu/uumemuv.tdcd:  Only hexlet stores were legal to NB; add octlet stores.
{cj,ife,tst}/*?rst.tst:  CPrdibtreq23 & CPwtibtreq5 were missing.
tst/drvchk.V:  Reg bypassing AUndx around SR pointing at stale name.
tst/job.tst:  Mask & div4 reversed for NB case of AUndx1500cR2.
euterpe.status:  CDIO fixed its write-hi-data-in hold violation a long time ago.
uu/uustepuu.pla:  Lessen confusion in comments on split-write ops (GGFMul/ExtrI)
----------------------------
revision 191.1
date: 1995/05/01 03:52:52;  author: mws;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/evblm.prio,v
Working file: verilog/bsrc/uu/evblm.prio
head: 131.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 131.9
date: 1995/05/04 07:24:56;  author: mws;  state: Exp;  lines: +50 -42
uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v
Working file: verilog/bsrc/uu/uu.V
head: 1.202
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 202;   selected revisions: 3
description:
issue unit
----------------------------
revision 1.186
```

```
date: 1995/05/04 07:25:02;  author: mws;  state: Exp;  lines: +8 -7
uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
----------------------------
revision 1.185
date: 1995/05/01 22:15:16;  author: woody;  state: Exp;  lines: +5 -3
euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.

icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 1.184
date: 1995/05/01 03:45:55;  author: mws;  state: Exp;  lines: +4 -3
uu/uumemuv.tdcd:  Comment:  explain why we don't improve the espresso phase.
uu/uu.V euterpe.V at/at.V uu/uu_control.pim:
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
  AT placement not updated but I think it was already not usable.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu_control.pim,v
Working file: verilog/bsrc/uu/uu_control.pim
head: 68.60
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 60;    selected revisions: 3
description:
----------------------------
revision 68.47
date: 1995/05/04 07:25:22;  author: mws;  state: Exp;  lines: +7 -4
uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
----------------------------
revision 68.46
date: 1995/05/01 22:15:37;  author: woody;  state: Exp;  lines: +1 -0
euterpe.V,at.V,atpadcd.Veqn,cc.V,ccstart.Veqn,uu.V:
Added illgToNb. This is a new exception 11 case. This term is intended to be
asserted for synch ops to nb and less then octlet stores to nb.

placement updated.
```

```
icachenoalloc, dcacheharder4 fabbed.
----------------------------
revision 68.45
date: 1995/05/01 03:46:13;  author: mws;  state: Exp;  lines: +16 -11
uu/uumemuv.tdcd:  Comment:  explain why we don't improve the espresso phase.
uu/uu.V euterpe.V at/at.V uu/uu_control.pim:
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
  AT placement not updated but I think it was already not usable.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uumemuv.tdcd,v
Working file: verilog/bsrc/uu/uumemuv.tdcd
head: 63.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 2
description:
----------------------------
revision 63.15
date: 1995/05/01 03:46:25;  author: mws;  state: Exp;  lines: +6 -1
uu/uumemuv.tdcd:  Comment:  explain why we don't improve the espresso phase.
uu/uu.V euterpe.V at/at.V uu/uu_control.pim:
  Split vldNoXcR10 to AT into a "vld for mem access" (keeping old name) & a "vld
  for causing xcptn" (new uu.vldOutR11/at.vldForXcR11) so that ifetch xcptns can
  freeze their LVA but not fetch memory.  Test icache_except(_0?) noticed.
  AT placement not updated but I think it was already not usable.
----------------------------
revision 63.14
date: 1995/04/30 08:18:12;  author: mws;  state: Exp;  lines: +5 -4
Only hexlet stores were legal to NB; add octlet stores.  Fix placement later.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uuprblmr11.Veqn,v
Working file: verilog/bsrc/uu/uuprblmr11.Veqn
head: 50.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 50.10
date: 1995/05/04 07:25:34;  author: mws;  state: Exp;  lines: +48 -16
uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uurst.tst,v
Working file: verilog/bsrc/uu/uurst.tst
head: 15.30
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 30;    selected revisions: 1
description:
----------------------------
revision 15.30
date: 1995/05/04 07:25:35;  author: mws;  state: Exp;  lines: +2 -2
uu/uuprblmr11.Veqn uu/uuprblmr11.Veqn uu/uu.V uu/uu_control.pim uu/evblm.prio \
at/at.V at/atxcfrz.Veqn at/at.pim euterpe.V:
  Replace uu.vldOutR11/at.vldForXcR11 (which was on so much it would allow
  hiccups to freeze the exception LVA) with uu/at.vldForFrzLvaR12 which tries
  to keep enabling of AT to freeze of xc LVA consistent with prblm priorities.
  Found by inspection (thanks woody), seems no test coverage.
{cj,rg,uu}/*?rst.tst tst/drvchk.V:  Add ATillglToNbR12 to match recent changes.
=============================================================================
```